

## Guidelines to Keep ADC Resolution within Specification

### 1. Introduction

This application note describes how to optimize the ADC hardware environment in order not to alter the intrinsic ADC resolution and to provide the best overall performance. Indeed, the resolution depends on both the ADC intrinsic noise and noise transmitted by an external environment such as package impedances, power-supply networks, de coupling networks, loops and antennas. Some electromagnetic mechanisms have to be known in order to improve immunity against radiated and conducted emissions. The environment noise level of a digital product is typically equal to +/-50mV. The resolution of 10-bit ADC is 4.88mV for a 5v voltage reference. Without any precaution up to four bits can be lost, thus degrading the ADC from 10-bits to 6-bits.

### 2. ADC Resolution

Two classes of noise can be defined in the ADC. The first is due to the conversion process called quantization and the second one is due the noise coming from the external environment of the electronic system.

#### 2.1. Quantization Noise

The ADC operation is an analog to digital conversion which translates an analog signal into a number called a digital sample as shown in Figure 1.

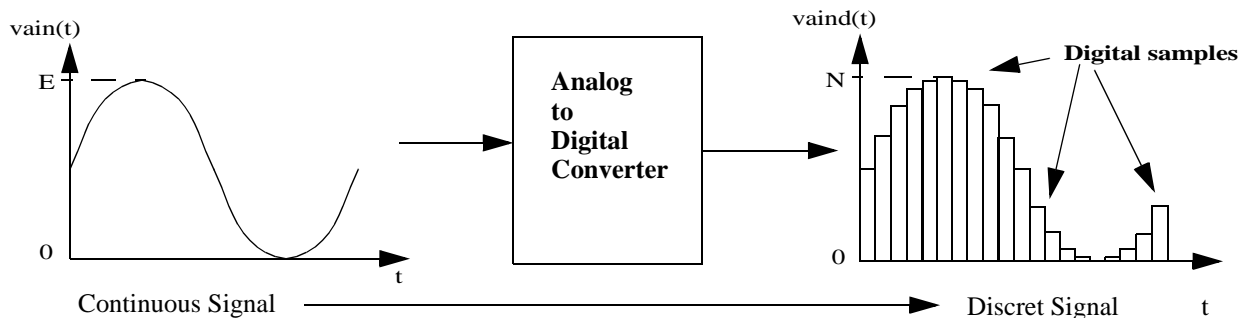


Figure 1. Analog to Digital process

This process is needed each time a continuous signal (**analog**) has to be handle by a digital system such as a computer. It can compute only discrete signals (**digital**). A continuous signal has an infinity of values. A discrete signal has only a finite number of values. A digital sample is an approximation of the continuous value. This approximation depends on the number of digital values that *vain* can take per sample. In other words it depends on the bit number used to code *vain* in digital format. The higher the number of bits, the better the approximation.

Table 1. Coding format

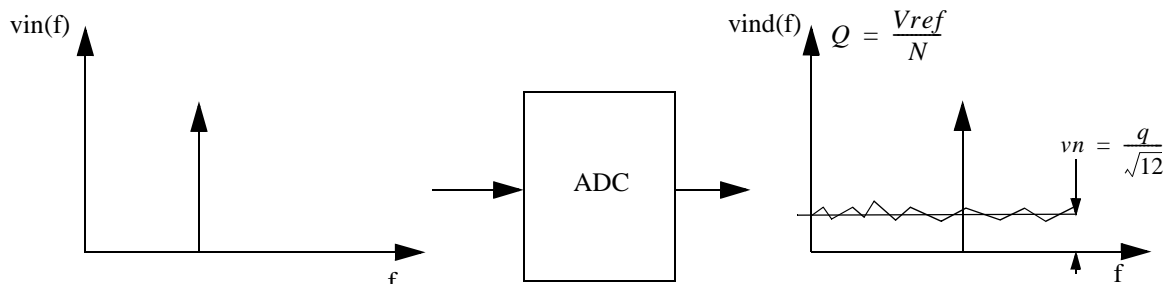
Number of bit	6	8	10	12
Number of digital value	64	256	1024	4096
Q(mV), Vref=5v	78.12	19.53	4.88	1.22

The quality of this approximation is defined as the ADC resolution. The higher the number of bits, the better the resolution. The resolution can be expressed in voltage and it corresponds to the smaller voltage which can be translated by the ADC. This minimum voltage is called voltage step or quantum (**Q**). It depends on the converter voltage reference (**Vref**) and the combination number (**N**):

$$Q = \frac{V_{ref}}{N}$$

Q which characterizes the conversion accuracy and is equal to  $\pm 1/2\text{LSB}$ . This conversion process is the first source of noise called RMS quantization noise  $vn$ .

It is shown in Figure 2 and is equal to: 
$$vn(V) = \frac{q}{\sqrt{12}}$$



**Figure 2. The ADC operation adds noise quantization**

Table 2 shows the quantum value and the quantization noise level according to the number of bits.

**Table 2. Quantum and quantization noise levels according to the bit number**

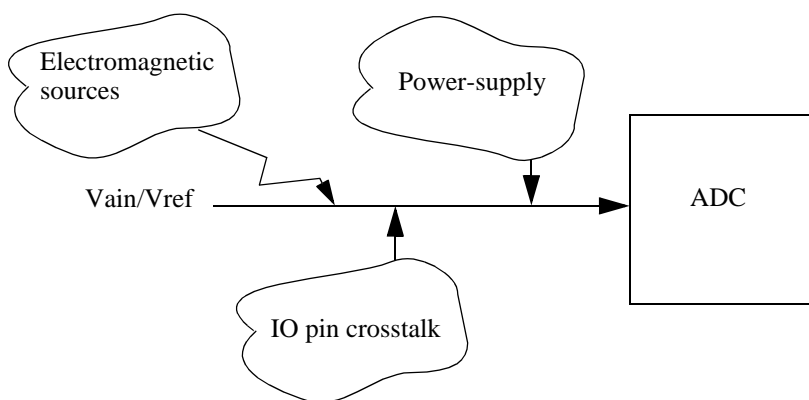
Number of bit	12	10	8	6
Q(mV)	1.22	4.88	19.53	7812
vn(mV RMS)	0.35	1.4	5.66	22.55

All values less than  $vn$  can not be converted because they are in the ADC noise floor.

## 2.2. External Noise Sources

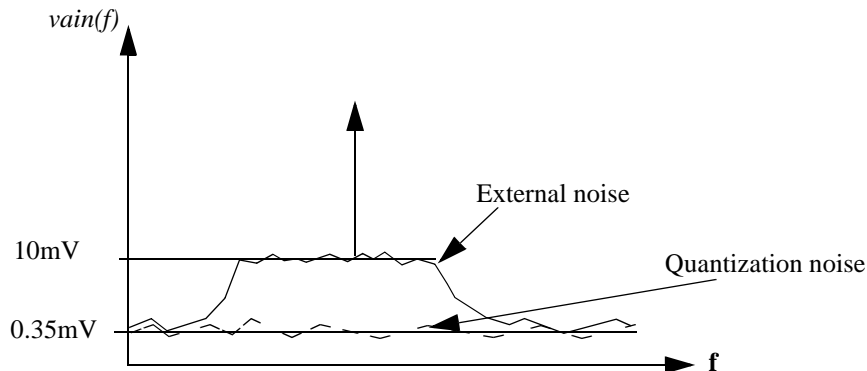
All the radiated and conducted emissions coupled to the  $vain$  and  $vref$  inputs can degrade the ADC resolution. Figure 3 shows three kinds of potential noise sources:

- the noise transmitted by the power-supply is totally rejected and a part of it is coupled to the ADC inputs,
- IO pins close to the ADC inputs are coupled through the package and a part of the switching current is transmitted to these ADC pins,
- radiated emissions are coupled to the ADC pins by the PCB tracks, loops and antennas.



**Figure 3. System noise floor affects the resolution**

Figure 4 illustrates the ADC resolution degradation when the external noise is not rejected enough. In this example the ADC has 12-bits and the RMS quantization noise level is 0.35mV.



**Figure 4. External noise degrades the 12-bit converter down to 9-bits**

The overall external noise level is evaluated at 10mV and the number of bits lost is:

$$2^N = 2^{\frac{10mV}{1,22mV}}, N = \frac{\log \frac{10mV}{1,22mV}}{\log 2} = 3$$

The ADC resolution is degraded and the new resolution is 9-bits instead of 12-bits. This example shows it is important to lower all the noise sources and to reduce all the coupling mechanisms in the electronic system in order to keep the ADC resolution in the specification.

This application note describes how to locate and to lower all these disturbances.

### 3. Basic Checklist For ADC Resolution Optimization

Some items have to be checked in order to keep the ADC resolution within specification:

- Analyze and locate noise sources and coupling mechanisms,
- Select the appropriate power-supply networks,
- Use the de coupling Strategy described inside,
- Use the smaller package,
- Use a package with separate power-supply Pins,
- Use separate analog and digital ground planes.

## 4. Noise Sources and Coupling Mechanisms

### 4.1. Typical ADC Application Description

Figure 5 shows a typical ADC application. The IC0 is an Atmel microcontroller including an ADC with an analog input (**Ain**) and a voltage reference input (**Vref**).

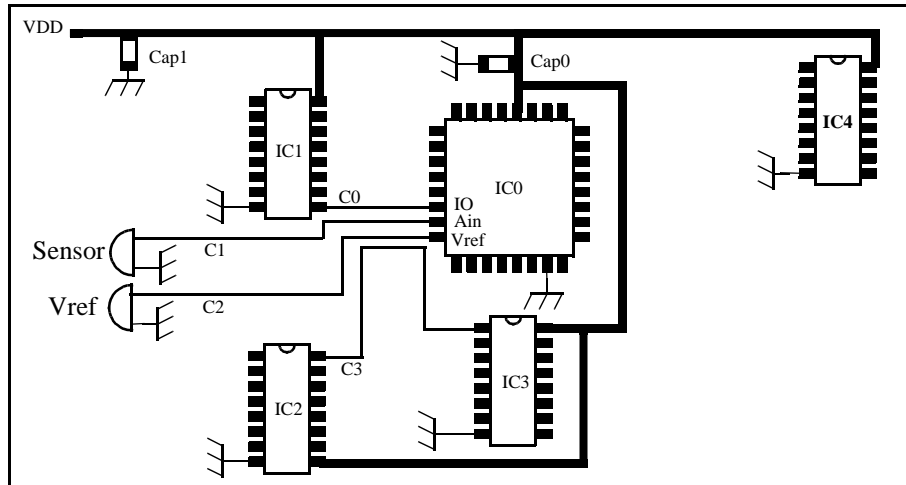


Figure 5. Typical ADC application

A sensor is connected to **Ain** and an external voltage reference to **Vref**. The IC1 is controlled by the IC0 IO pin. The IC2 and the IC3 are two external devices and one of the PCB connections is routed close to the **Vref** connection. The IC4 shares the common VDD.

### 4.2. Noise Source and Coupling Mechanism Analysis

#### 4.2.1. Conducted Mode Analysis

Figure 6 describes the main noise sources and the main coupling mechanisms in conducted mode and how they can influence the ADC resolution. These are detailed below:

- **vn4**: this noise is generated by all IC activities and is transmitted to the power-supply rails,
- **vn3, vn2**: this noise is generated by the internal logic activities and through the packaging impedances,
- **vn1**: a current flowing through the PCB connection from the IC2 to the IC3, induces a current and then the voltage drop **vn1** which is transmitted to the **Vref** input of the ADC comparator by magnetic coupling with the C2 connection,
- **vn0**: The IC0 generates a signal on the IO pin. There is a magnetic coupling of the package between the IO and the **Ain** pin. The current flowing into the IO pin induces a current due to the magnetic coupling into the **Ain** pin and causes the voltage drop **vn0** on this pin.

The combination of all these noise sources can affect the overall ADC resolution. An ADC operation is based on a voltage comparison between an analog signal and a programmable voltage reference. This comparison process is done until both comparator inputs are equal. The result is an integer value which reflects the analog value. If a noise is injected in one of both inputs the comparator result is affected and the digital value is corrupted by this noise. If the same noise is injected in both inputs, in differential, the noise contribution will be cancelled and the digital result will not be affected (common mode).

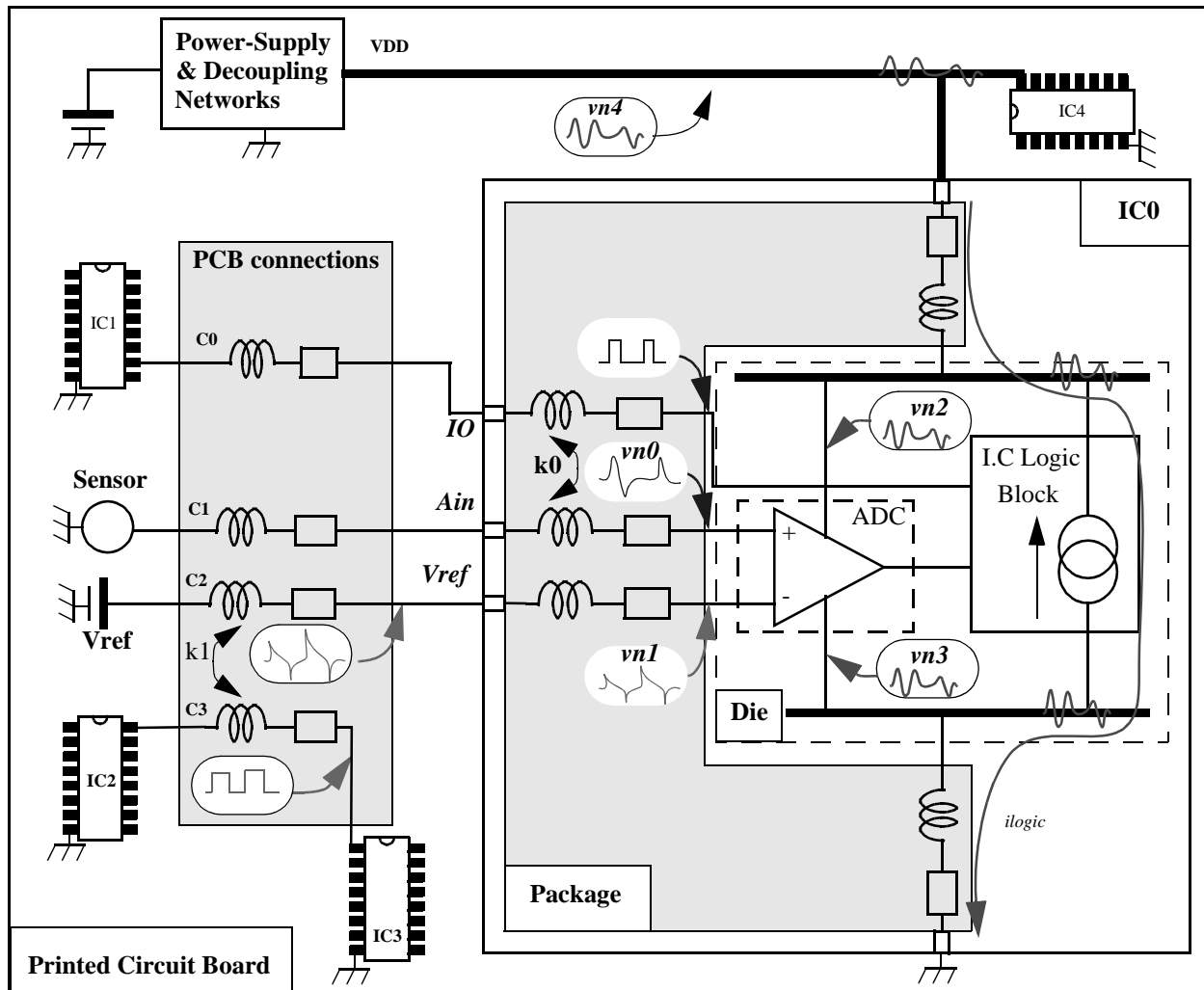


Figure 6. Noise sources and coupling mechanisms

#### 4.2.2. Radiated Mode Analysis

In this mode the PCB layout has to be checked in order to find the loops and wires that can act like antennas. In Figure 7 a PCB lay-out is given around the *Ain* input.

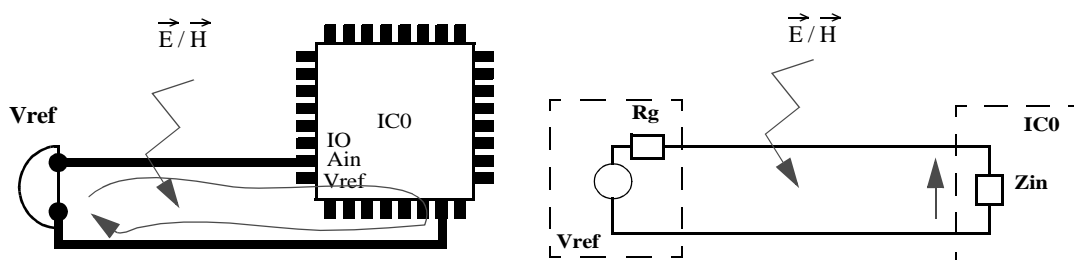


Figure 7. Loops and wires have to be analyzed to protect them against electromagnetic fields

This topology can be:

- a loop, if  $R_G + Z_{in}$  is low compared to the loop impedance (typically 100ohms),

- an antenna, if  $RG+Z_{in}$  is high compared to the loop impedance.

The PCB connection impedance varies according to the frequency as shown in Figure 8. In some bands the topology acts like an antenna and in other bands the topology acts like a loop. The topology impedance depends on:

- nature and thickness of the dielectric (epoxy, glass, ceramic, ...),
- the PCB track size (width, length, ...),
- the PCB structure (ground plane or not, power plane or not, ...).

## 4.3. Conclusions

The general concept to have the best ADC resolution is to lower the amplitude of all the noise sources. The power-supply network is the major contributor and its impedance has to be lowered to the minimum in the frequency band of the component. The coupling mechanisms have to be reduced and the connection impedance has to be lowered too.

## 5. Noise Optimization

To reduce the noise level of the overall system and obtain the best ADC resolution, each contributor has to be optimized. This chapter discusses how to optimize the noise sources (power-supply network and de coupling network) and the coupling mechanisms (package).

### 5.1. Power-Supply and Decoupling Networks

The power-supply network is a major contributor for the noise generation and it is important to maintain its impedance low especially in the frequency bands where the system operates. The decoupling network helps to reduce this impedance in the frequency band where the IC operates (see application note ANM85).

#### 5.1.1. Power-Supply Network

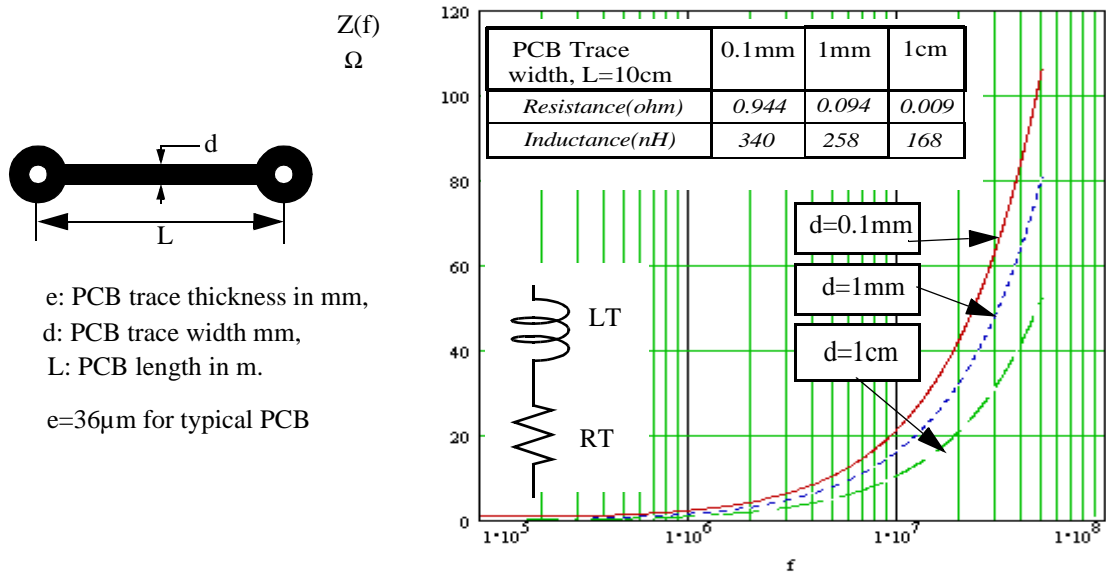
Several topologies can be used to implement the power-supply. The impedance across power pins can vary from a few ohms to a hundred ohms:

- PCB tracks,
- One layer for ground and PCB tracks for the power,
- Double layers for ground and power.

The choice of the topology is led by the price, the operation frequency and the protection against the internal and external disturbances. When there is no constraint in terms of emission and/or immunity, simple PCB tracks can be used to power the application. A double layer connection is advised when the system operates in high frequency and when the system is in a disturbed environment. To analyze the influence of the topology on the connection inductance, the path of the return current has to be taken into account to calculate the global inductance of the PCB connection.

##### 5.1.1.1. PCB tracks

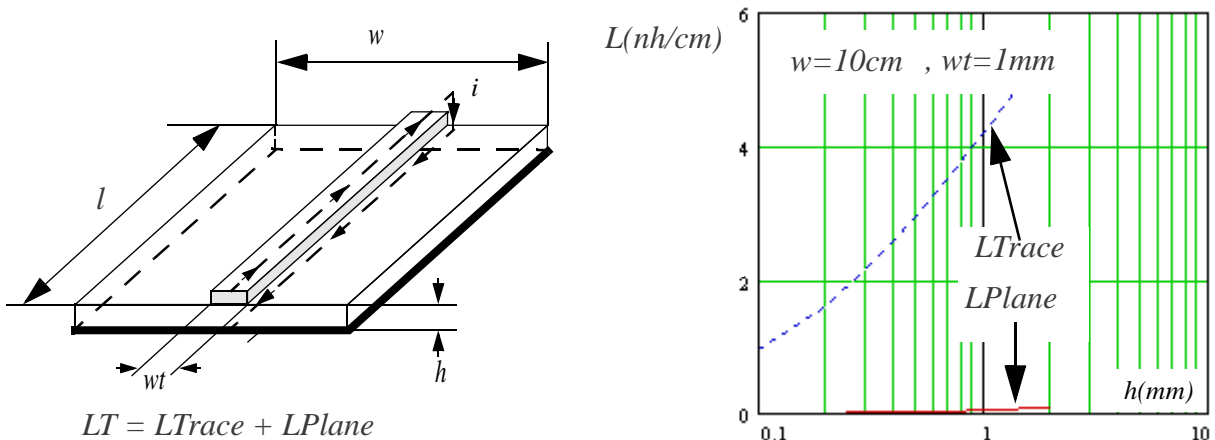
A connection can be modeled by a RL model as it is shown in Figure 8. In low frequency the connection is a pure resistor and in high frequency it is an inductance. The wider the PCB trace width, the lower the inductance.



**Figure 8. A PCB connection is a RL model**

**5.1.1.2. One layer for ground and PCB tracks for the power**

If the PCB connection is too inductive, a ground layer allows to lower the inductance value of the return current. A PCB connection is typically 5nH/cm and 0.8nH/cm for a ground plane layer.

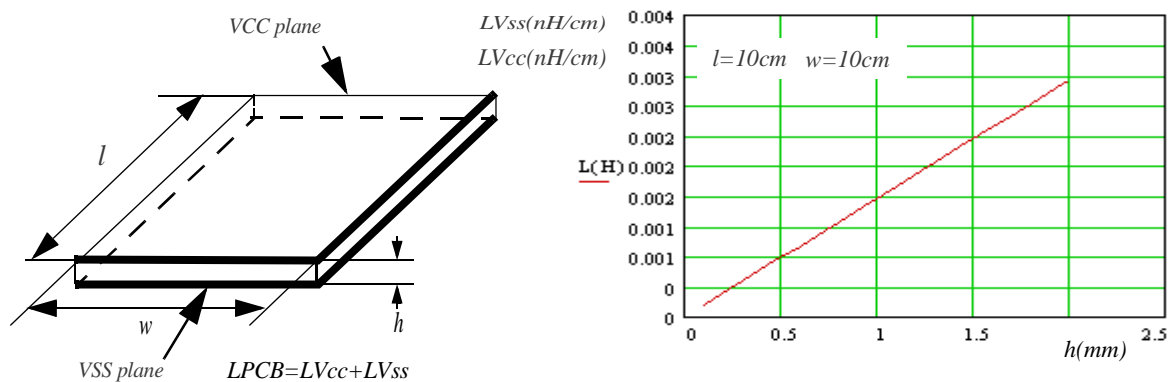


**Figure 9. A ground layer lowers the inductance value of the PCB connection**

Figure 9 gives both inductance values for the PCB connection implemented above a ground plane and the inductance of the ground plane

**5.1.1.3. Double layers for ground and power**

If the inductance is still too large, a double plane has to be used. The inductance for both Vss and Vdd plane is around 2.5pH/cm.



**Figure 10. A double copper plane is the lowest inductance topology.**

Figure 10 plots the inductance value of the VCC and VSS ground planes according to the PCB thickness. It is the best topology to reduce the emission levels and to improve the immunity.

### 5.1.1.4. Comparison between the three cases described above.

Table 3 gives a comparison between all the three configurations analyzed above.

**Table 3. Comparison of the PCB inductance for w=1mm, wt=10cm, l=10cm, h=1.6mm**

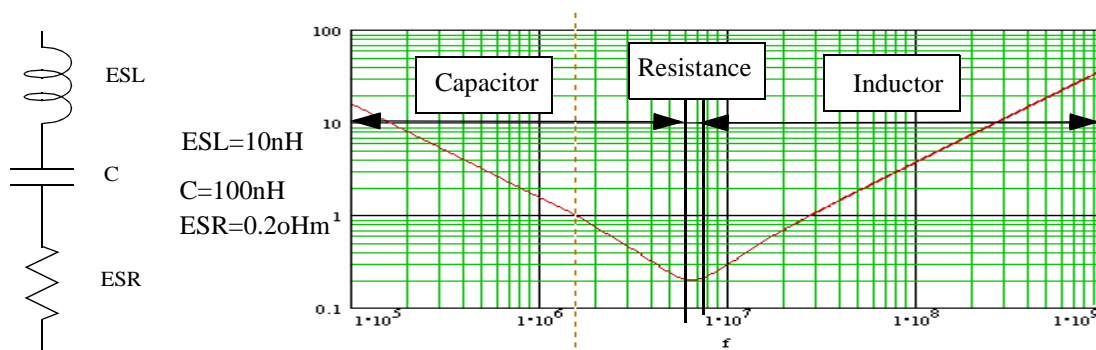
	Vcc PCB trace Vss PCB trace	Vcc PCB trace Vss plane	Vcc Plane Vss Plane
Inductance(nH)	115 + 115=230	51 + 0.8=51.8	0.025 + 0.025=0.05
Capacitance(pF)	5pF	20pF	271pF

The global inductance of a PCB connection with its return current connection is 406 higher than its equivalent double plane topology.

### 5.1.2. Decoupling Network

The role of the decoupling network is to stabilize a power-supply network and to lower the power impedance in the operation frequency bands of the system by:

- maintaining a low impedance across the power-supply pins of ICs in the frequency range of operation,
- stabilizing the connections on the wiring connected between the power-supply equipment and the electronic system equipment.



**Figure 11. Capacitor impedance according to the frequency.**



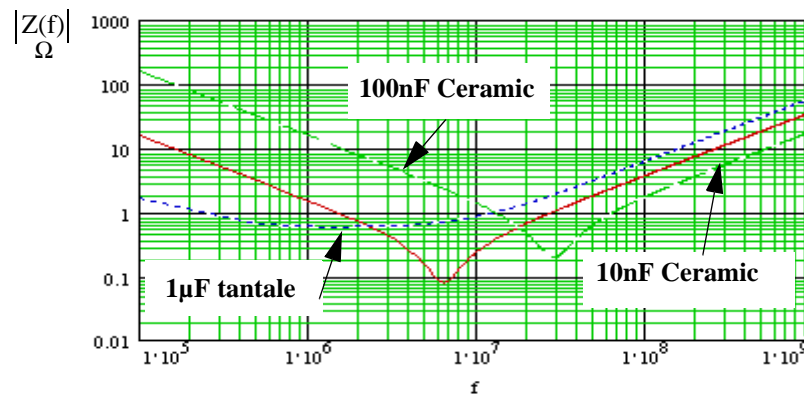
The decoupling network uses some decoupling capacitors. The impedance of a pure capacitor decreases when the frequency increases. But a capacitor is not a pure one. It consists of some parasitic elements such as an inductor (ESL) and a resistor (ESR). So the capacitor model is a RLC circuit. The behavior of such a model according to the frequency is shown in Figure 11.

The equivalent inductance is the sum of the intrinsic inductance of the capacitor and the inductance of the connection. Table 4 shows the RLC model for different capacitor technologies.

**Table 4. Capacitor characteristics comparison.**

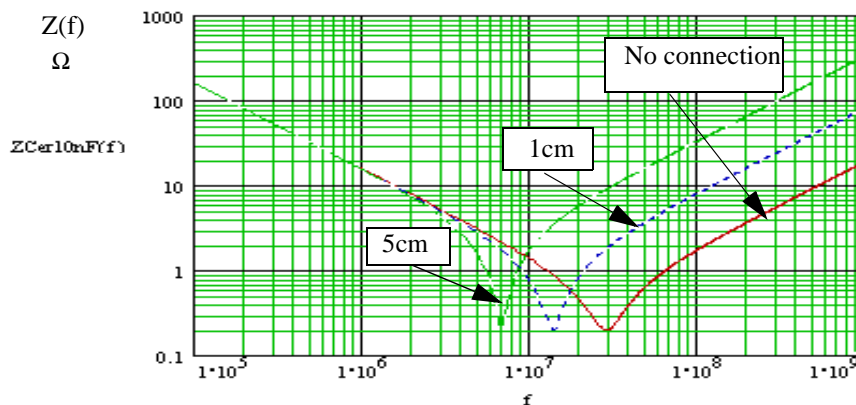
	1 $\mu$ F Tantale	100nF Ceramic	10nF Ceramic
R	0.8	0.08	0.2
L(nH)	6	3	3
Fr(MHz)	2	7.1	29

Figure 12 plots the capacitor impedance according to the frequency and the capacitor values.



**Figure 12. The capacitor impedance is according to the capacitor values.**

Figure 13 plots the capacitor impedance according to the connection length between the capacitor and the power pins. The longer the connection, the higher the inductance. The resonance varies from 7MHz to 30MHz when the connection length varies from 0 to 5cm.



**Figure 13. The capacitor impedance according to the connection length.**

Figure 14 shows a way to reduce the impedance by putting several identical capacitors in parallel.

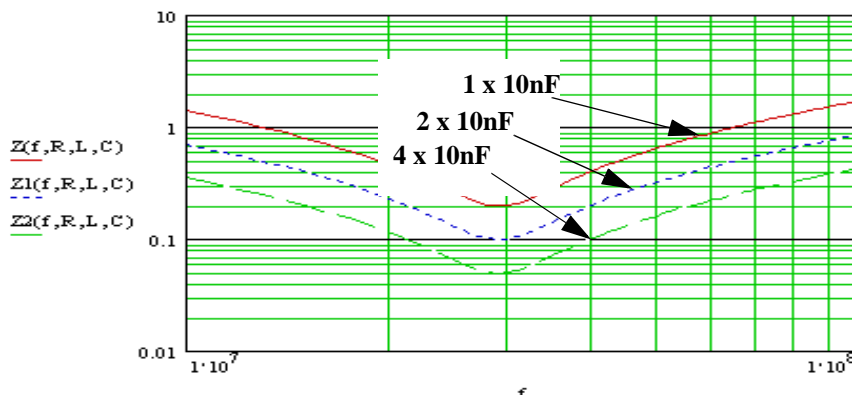


Figure 14. Several identical capacitors helps to lower the impedance value.

### 5.1.3. Decoupling Strategy

The role of decoupling capacitors is to maintain a low impedance across ICs. A digital IC works synchronously to a clock and therefore most of the dynamic currents are synchronized to that one. A decoupling capacitor has to be tuned around that clock frequency in order to short-circuit the disturbance synchronous to the clock. To do this, the RLC model of the connection taken between the VDD and the VSS pins has to be evaluated. The equivalent inductance is the sum of LC, LP2 and LP1.

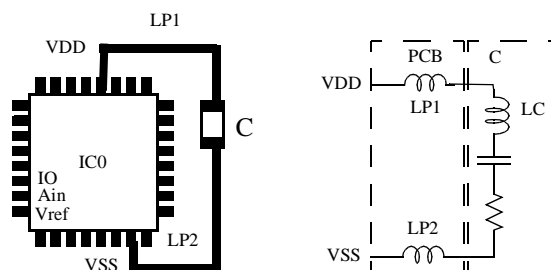


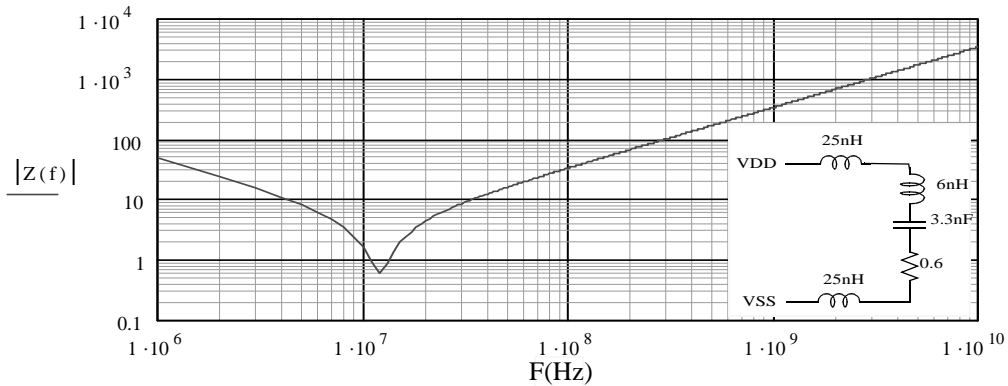
Figure 15. Electrical model of the basic decoupling network.

If the clock frequency is  $F_0$ , then the decoupling capacitor can be evaluated by the formula shown below:

$$C = \frac{1}{(2 \times \pi \times F_0)^2 \times (LP1 + LP2 + LC)}$$

The parasitic inductances depend on the decoupling capacitor types and the PCB topology chosen. For example, the capacitor is a SMD type and the intrinsic inductance is 6nH. The PCB has no power planes, the PCB connection inductances are 10nH/cm and the total connection length is 5cm, therefore  $LP1+LP2=50nH$ . The clock is 12MHz and C is equal to 3.3nF.

Figure 16 plots the impedance for a 3.3nF capacitor and the 56nH parasitic inductance. This capacitor value ensures a minimum of impedance around the 12MHz clock frequency. The fast digital currents are frequently a broad band signal and it is necessary to maintain a low impedance until the 100MHz band. To do this, some decoupling capacitors are added and if the double power plane topology is chosen a pure HF capacitor should be added. The values are evaluated on the third overtones of the clock frequency but should be adapted to the shape of the VDD current.



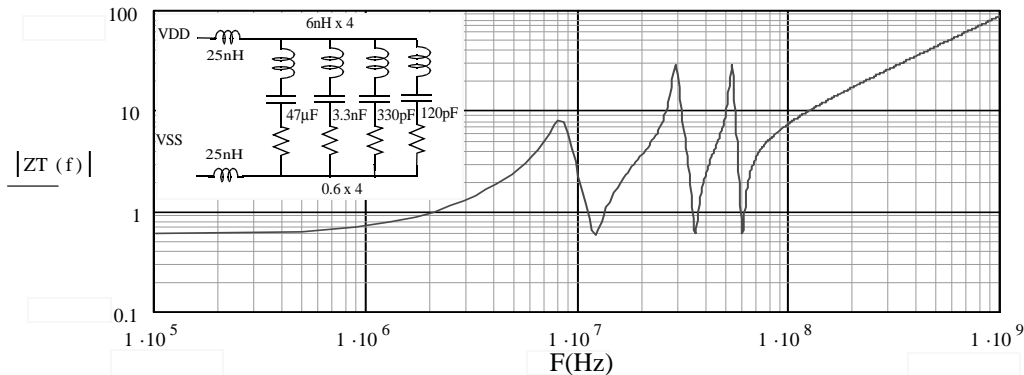
**Figure 16. Frequency response of the power-supply network.**

**5.1.3.1. PCB Track Topology**

Figure 17 plots the network impedance based on the rule mentioned above. The decoupling capacitors are connected to the VDD and the VSS pins by two PCB tracks. The decoupling capacitor values are given in Table 5.

**Table 5. Decoupling capacitor values**

100KHz	12MHZ	36MHZ	60MHZ
C0=47 $\mu$ F	C1=3.3nF	C2=330pF	C3=120pF



**Figure 17. Power-supply network Impedance for PCB connections without ground plane.**

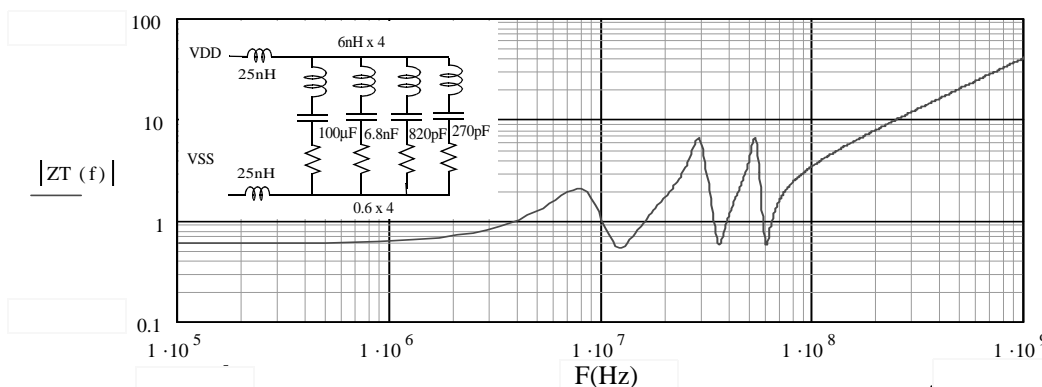
The impedance is maintained below 30ohms from 100KHz to 100MHz. With such a topology, it will be impossible to lower the impedance more above 200MHz because the inductance connection causes a high impedance in the VHF/UHF band. At 1GHz the impedance is below 80 ohms.

**5.1.3.2. One Ground Plane layer and PCB tracks**

Figure 18 plots the impedance network for ground plane topology and for the decoupling capacitors given in Table 6

**Table 6. Decoupling capacitor values.**

100KHz	12MHZ	36MHZ	60MHZ
C0=100 $\mu$ F	C1=6.8nF	C2=820pF	C3=270pF



**Figure 18. Power-supply network impedance for a ground plane topology.**

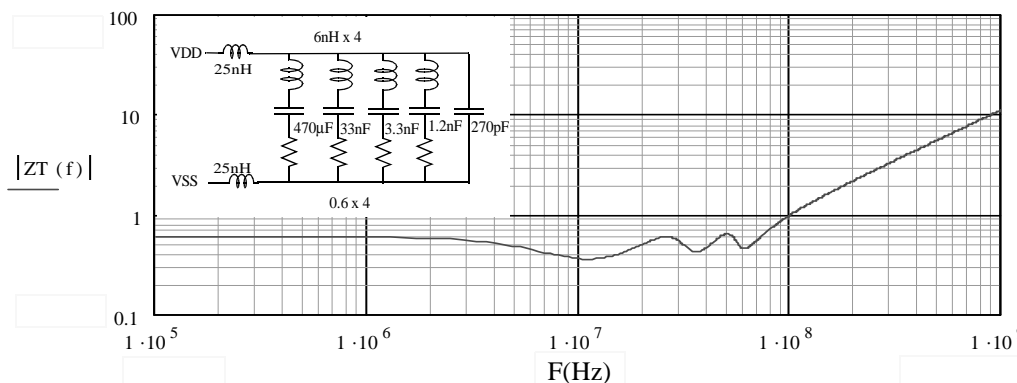
The impedance is maintained below 6 ohms from 100KHz to 100MHz. Compared to the first topology, this ground plane divides the network impedance by five. As the first topology it will be impossible to reduce the impedance more in the VHF/UHF band. At 1GHZ the impedance is below 40ohms.

### 5.1.3.3. Double Layers for VDD and VSS

Figure 19 plots the impedance network for ground plane topology and for the decoupling capacitors given in Table 7. The PCB capacitor is efficient in high frequency and not in low frequency because in this range the impedance is too high. It is necessary to have additional decoupling capacitors.

**Table 7. Decoupling capacitor values.**

100KHz	12MHZ	36MHZ	60MHZ	PCB capacitor
C0=470μF	C1=33nF	C2=3.3nF	C3=1.2nF	270pF



**Figure 19. Power-supply network impedance for a double plane topology.**

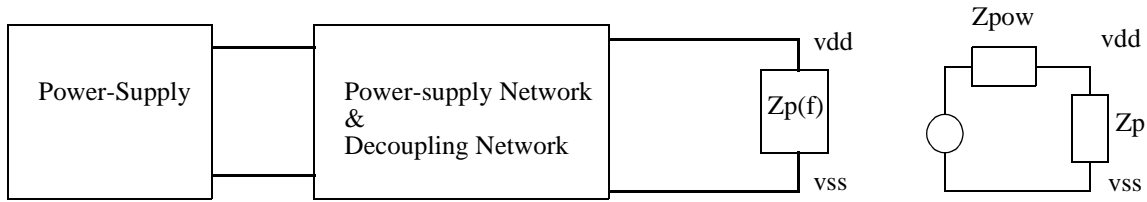
The impedance is maintained below 1 ohm between 100KHz to 100MHz. Thanks to the capacitor built with the double plane of the PCB, the impedance in the VHF/UHF band in reduced down to 10 ohms. This topology lowers the resistance and the inductance to the minimum.

## 5.2. Package Type

The package is the second major contributor and contributes to increasing the noise level. The package is similar to an impedance and is a load to the power-supply network as it is shown in Figure 20. The voltage variation across the package depends on  $Z_{pow}(f)$  and  $Z_p(f)$ :

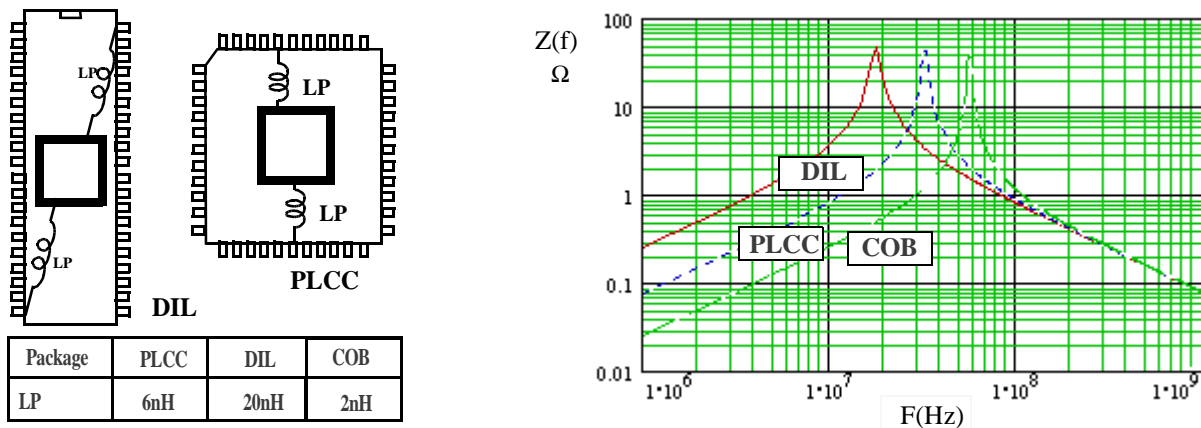
$$v_{dd} = VDD \times \frac{Z_p}{Z_P + Z_{pow}}$$

The lower the package impedance, the lower the  $v_{dd}$  variation.



**Figure 20. The package impedance increases the noise level.**

The package connection consists of a lead-frame (package lay-out) and bond-wires. The power-supply pins act as a magnetic loop or as an antenna. The bigger the package, the higher the Q factor thus the impedance

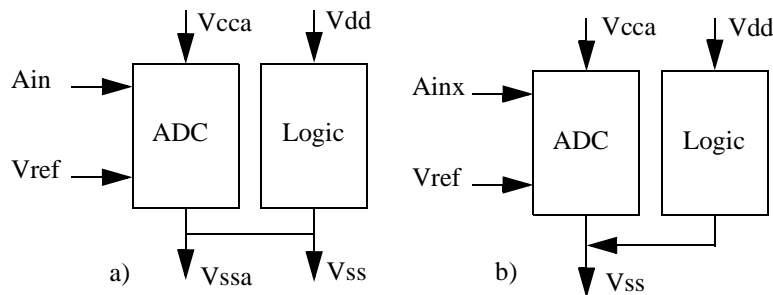


**Figure 21. Package impedance according to the package type and frequency.**

Figure 21 plots the impedance and the Q factor for three package types. Therefore it is recommended to use the smallest package in order to reduce the impedance and the topology antenna in the frequency band where the electronic system works.

### 5.3. Power-Supply Pin Configurations

Two kinds of configuration for the ground pin can be found and are shown in Figure 22. The first one has two separate pins (Figure 22.a), one for the analog and one for the digital. The second one has only one ground pin (Figure 22.b).



**Figure 22. Power-Supply pin Configurations**

To evaluate the performance of these configurations, the voltage difference between the *Ain* and *Vref* inputs has to be evaluated. Indeed, the conversion process translates this voltage difference. The noise affects the conversion result only if both inputs don't receive the same noise level value.

### 5.3.1. Common Ground pin

In this configuration shown in Figure 23, there is a common ground pin for both analog and digital ground pins.  $Z_p$  is the package impedance of the VSS pin. The package impedance of the *Ain* and *Vref* inputs is shown in the electrical schematic.  $Z_{ain}$  and  $Z_{ref}$  are the input impedances of the ADC. Logic activities create large digital currents, *iDigital*, which generate a noise level across the package impedance. The analog current, *iADC*, is negligible compared to *iDigital*.

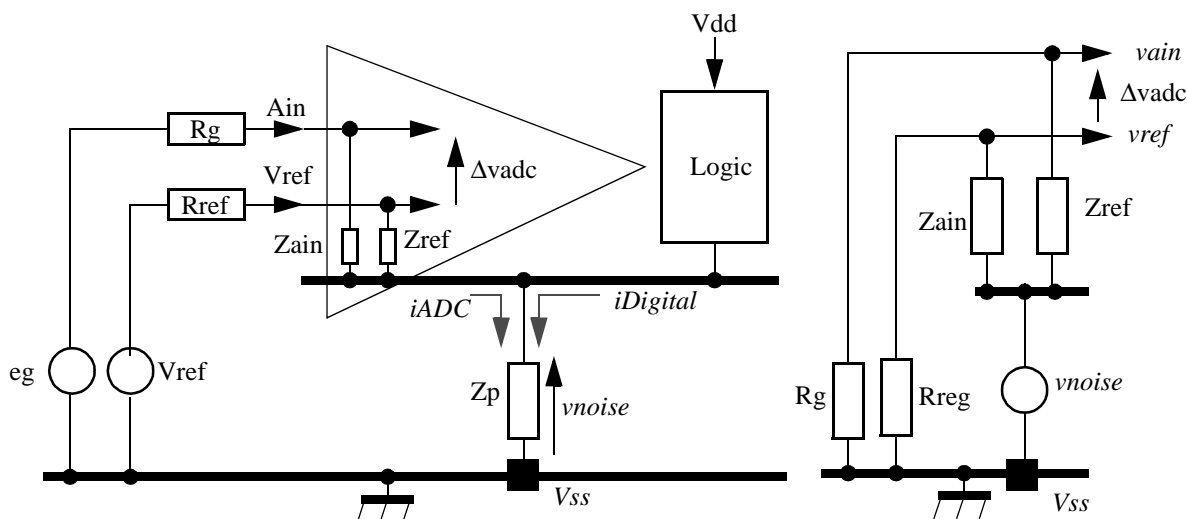


Figure 23. Equivalent electrical schematic for a common ground pin.

The input voltage, *vain* and *vref*, can be expressed according to the noise source with the formula shown below:

$$v_{ain} = v_{noise} \times \frac{r_g}{r_g + Z_{ain}}, v_{ref} = v_{noise} \times \frac{R_{ref}}{R_{ref} + Z_{ref}}$$

The next formula is used to evaluate the voltage difference between *vain* et *vref*:

$$\Delta v_{adc} = v_{ain} - v_{ref} = v_{noise} \times \left( \frac{R_g}{R_g + Z_{ain}} - \frac{R_{ref}}{R_{ref} + Z_{ref}} \right)$$

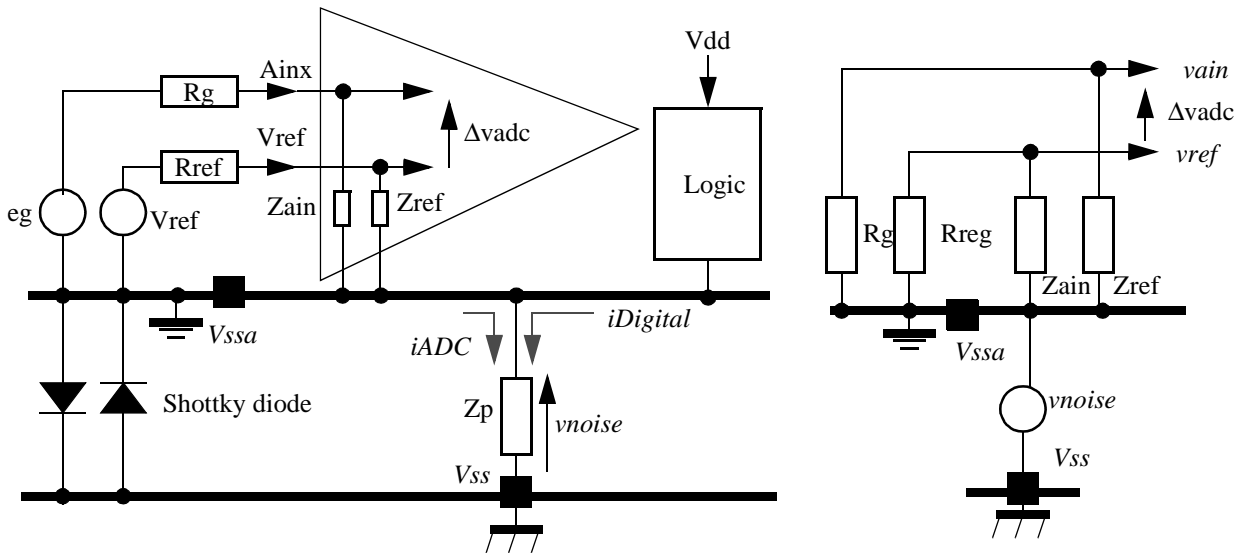
Finally, to improve the ADC immunity, both terms shown below have to be equal:

$$\frac{R_g}{R_g + Z_{ain}} = \frac{R_{ref}}{R_{ref} + Z_{ref}}$$

Typically, both sensor and voltage reference impedances as well as both *vref* and *ain* inputs have to be equal. In this case the noise generated by the digital activities does not affect the ADC resolution.

## 5.3.2. Dedicated Analog and Digital Ground Pins

In this configuration, the analog and digital grounds are separated.  $Z_p$  is the package impedance of the  $V_{ss}$  pin. The package impedance of the  $A_{in}$  and  $V_{ref}$  inputs as well as  $V_{ssa}$  are not taken into account.



**Figure 24. Equivalent electrical schematic for analog and digital ground pins.**

With such a configuration, the switching noise is not transmitted to the ADC inputs and gives the best immunity. Two Shottky diodes are inserted to prevent accidental voltage (DC, ESD, ..) from developing between the two ground systems.

## 6. Conclusions

The environment noise level of a digital product is typically equal to +/-50mV. The resolution of a 10-bit ADC is 4.88mV for a 5v voltage reference. Without any precaution, typically up to 4 bits can be lost, thus degrading the ADC from 10-bits to 6-bits. In other hand, keeping both the network and the IO interface impedance low allows to maintain a 9 to 10-bit resolution. This is why it is important to analyze and to optimize the power-supply and decoupling networks as well as the IOs interfaces.

## 7. References

- Controlling Radiated emissions by design, Michel Mardiguian, Chapman&Hall,
- Printed Circuit Board Design Techniques for EMC Compliance, Mark I.Montrose, IEEE Press,
- Noise Reduction Techniques In Electronics Systems, Henry W. Ott, Wiley Interscience.
- Application Note, ANM085, EMC Improvement Guidelines, Atmel-wm, Jean-Luc Levant